

G. KULESZA-MATLAK<sup>\*\*</sup>, K. GAWLIŃSKA\*, Z. STAROWICZ\*, A. SYPIEŃ\*,  
K. DRABCZYK\*, B. DRABCZYK\*, M. LIPIŃSKI\*, P. ZIĘBA\*

## BLACK SILICON OBTAINED IN TWO-STEP SHORT WET ETCHING AS A TEXTURE FOR SILICON SOLAR CELLS – SURFACE MICROSTRUCTURE AND OPTICAL PROPERTIES STUDIES

In this study a two-step short wet etching was implemented for the black silicon formation. The proposed structure consists of two steps. The first step: wet acidic etched pits-like morphology with a quite new solution of lowering the texturization temperature and second step: wires structure obtained by a metal assisted etching (MAE). The temperature of the process was chosen due to surface development control and surface defects limitation during texturing process. This allowed to maintain better minority carrier lifetime compared to etching in ambient temperature. On the top of the acidic texture the wires were formed with optimized height of 350 nm. The effective reflectance of presented black silicon structure in the wavelength range of 300-1100 nm was equal to 3.65%.

*Keywords:* black silicon, low temperature texturization, silicon nanowires, solar cells, multicrystalline silicon

### 1. Introduction

After many years of expansion of new photovoltaic (PV) technologies and different types of solar cells, it is clearly visible that silicon still has undeniably strong position in PV market [1]. The European investors are continuously choosing mostly silicon-based photovoltaic plants, mainly multicrystalline (mc-Si). In comparison to the fresher PV technologies e.g. newest perovskite trend, crystalline silicon solar cells still seem to be irreplaceable. Unfortunately, the mentioned perovskite technology, although very interesting and fast growing, does not guarantee a long-term stability and many years' power guarantee [2]. Therefore, silicon technology remains in the interest of researchers, who investigated each single component of the silicon solar cell.

This paper is about reducing the reflectance from the front side of silicon solar cell, which leads to the increase of solar radiation involved in the photovoltaic conversion. For this purpose, the surface texture is produced on the top of wafer, which leads to the reflectance reduction by the multiple reflection (at least twice). The silicon texture formation processes can be divided into two groups. To the first group belong methods which are precise and provide to significant reductions in reflectance, but are expensive and time consuming. Among those methods we can distinguish laser structuring [3-4], plasma treatment [5], reactive ion etching with or without masking [6-9] and electrochemical treatment [10]. In opposite to them, the wet chemical methods are most commonly used in mass production. Generally, acidic texturing discovered in the fifties of the twentieth century [11-14] is still used for mc-Si wafers, what is considered to be

exceptionally fast and cheap. Even nowadays, a lot of papers are published which report the mechanisms of reaction and etched pits formation [15-18]. Moreover, the authors of presented paper were also involved in the intensive investigation of porous silicon formation and acidic texturization mechanisms [19-24].

Apart from one-step texturing, it is interesting to go one step further and a black silicon creating with nanowires formation on the top of surface texture. Various methods have been developed to fabricate Si nanostructures in top-down or bottom-up scheme. Among them, metal-assisted chemical etching (MAE) is particularly intriguing and promising, because of its simplicity, good cost-efficiency, and versatility [25-29]. In a model describing MAE process, the oxidant is preferred to be reduced at the surface of metal catalyst, and holes (h<sup>+</sup>) are injected from metal catalyst to Si or electrons (e<sup>-</sup>) are transferred from Si to metal catalyst. Si underneath metal catalyst has the maximum hole concentration, therefore the oxidation and dissolution of Si occur preferentially underneath metal catalyst [25]. Nanowires may be formed on polished silicon wafers. Generally, the critical factors are height of a structure [30] and roughness which influence the effective charge carrier lifetime and thus the efficiency of solar cell [31-32]. It became popular to etch wires on pyramidal textures [33] or pyramids on the wires [34]. It was reported that wires are effective in combination with acidic texture on multicrystalline silicon. Initially, wires were made from another material such as ZnO [35], then they were performed by etching of silicon but more in form of porous material than wires [36] and finally wires on the pits-like structure [37]. In the case of such structures, a great attention is paid to the correct selection

\* INSTITUTE OF METALLURGY AND MATERIALS SCIENCE OF POLISH ACADEMY OF SCIENCES, 25 REYMONTA STR., KRAKOW, POLAND

# Corresponding author: g.kulesza@imim.pl

and performance of surface passivation [38-41] (with or without anti-reflective coating) and metallic contacts [42].

This paper discusses the problem of black silicon structure formation consisting of wires with different height on the silicon wafer with polished surface or textured in acidic or alkaline solutions. The novelty of this work is the combination of wires with acidic texture obtained at low temperature, which provides excellent optical properties while maintaining good carrier lifetime.

## 2. Experimental

Silicon wafers used in the experiments were 'as cut', p-type, 0.5-3 Wcm multicrystalline silicon wafers 'Swiss Wafers BG', square shape 25 cm<sup>2</sup> and 200 μm thick. The initial preparation of samples consisted of surface mechanical washing in propanol and acetone. Afterwards, wafers were subjected to cleaning at first in acetone and subsequently in propanol bath at elevated temperature.

The black silicon was prepared in two-step procedure starting from acidic texturization and ending with wires formation. Generally, both processes were performed in chemical bath to get low production cost, fast delivery time and leave a possibility to implement in the production line. Special care was taken to proper cleaning of the samples by rinsing in deionized (DI) water and thoroughly drying.

### First step: texturization process

The texturization process was carried out in acidic solution containing hydrofluoric (40% Chempur pure p.a.) and nitric (65% Chempur pure p.a.) acids. For this investigation also DI water was added to control the concentration of etching medium. To determine the best composition of the texturing solution the previous, own research has been exploited [18,19]. In brief, the composition was specified using a concentration triangle and finally, the concentration HF:HNO<sub>3</sub>:H<sub>2</sub>O = 8:1:1 in volume ratio was selected. Both time and temperature of texturization affected a formation of proper texture with regular pits and reduction of etched defects located on the wafers surface. In this case a selected process time was equal to 60 seconds. Temperature of the process was reduced by cooling of the substrates and performing whole etching in tanks surrounded by ice. The temperature of texturing medium increased from 10°C to 12°C during whole 60 seconds of texturing.

### Second step: wires formation

Silicon nanowires were formed on the wafers with isotropic texture by metal assisted etching (MAE) with silver as a catalyst. At first, a thin layer of naturally formed silicon dioxide was removed in the 5M HF bath which resulted in the hydrophobic surface of wafer. Subsequently, dipping in methanol was performed to return to hydrophilic state of wafer surface. The proper wires formation started with silver deposition from 0.02M aqueous solution of silver nitride (>99.8% Sigma-Aldrich pure p.a.) in DI water, acidified with 5M HF in volume ratio 1:1. The

time of dipping was set to 20 seconds and provide to the silver nanoparticles structure formation presented in Fig. 1.

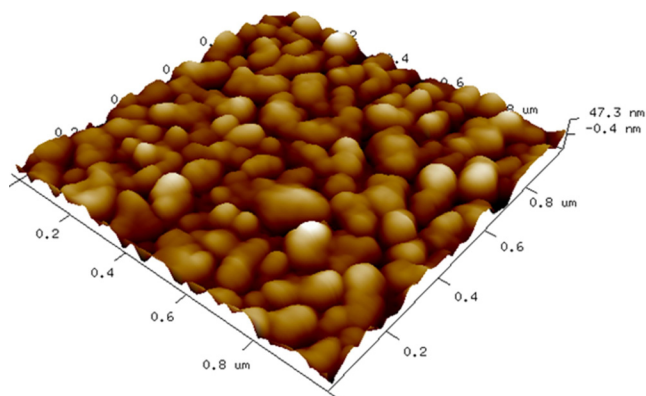


Fig. 1. AFM image of silver nanoparticles deposited from acidified aqueous solution of silver nitride in DI water on chemically polished monocrystalline silicon wafer

Then, the etching process was carried out in HF:H<sub>2</sub>O<sub>2</sub> solution with 10:1 volume ratio in different periods of time. For accurate determination of wires morphology and length, etching was also performed on monocrystalline silicon (Czochralski, p-type, 0.5-1 Wcm, pseudo-square shape 25 cm<sup>2</sup> and 200 μm thick) which was chemically polished in 30% KOH solution (85% POCH pure p.a.) at elevated temperature. The thickness of removed layer was at least 15 μm per each side. Additionally, the structure of wires was etched out on the textured surface which was etched in a solution of KOH:IPA:H<sub>2</sub>O(DI) = 1:3:46 in volume ratio, temperature in the range 78-82°C and time equal to 40 minutes.

The surface morphology was examined using scanning electron microscopy (SEM) technique using QUANTA 200 3D Dual Beam (FEI) and TM3030 Tabletop Microscope (HITACHI). A Lambda 950S spectrometer with integrating sphere (Perkin Elmer) was used to measure the surface reflectivity. The wafers topography (roughness and profiles) was measured by atomic force microscopy technique using Innova Veeco system (Bruker). The minority carrier lifetime was examined using WCT-120 QSSPC system (Sinton Consulting).

## 3. Results and discussion

The mc-Si wafers are typically textured in the acidic solution. Because the polycrystalline wafer contains grains of different surface orientation, and thus different atom surface density, one cannot say that the texture obtained by the chemical etching is identical in each place. However, for the sake of simplicity it is assumed that we are dealing with completely isotropic texture. Selection of the appropriate composition, time and temperature of the process were included in other authors' papers [18,19]. Here, a well-known process was proposed where the solution content was as follows HF:HNO<sub>3</sub>:H<sub>2</sub>O = 8:1:1 in volume ratio. This resulted in a characteristic pits-like morphology of oval

shape and gentle slopes. In most cases the cross-section of the pit can be described as a circle cut. Besides the concentration, two other factors influence surface topography: time of the process and temperature of the etchant. Moreover, modifying both of them the similar surface morphology was obtained but the mechanism of surface structuring proceeded differently. Time reduction could be a limiting factor in pits development while the temperature decrease reduces the reactivity of chemical etching. Finally, the proper texture with good opto-electronical properties was received using composition described above for time equal to 60 second at temperature of 10-12°C. The surface morphology of the silicon wafer with acidic texture at lower temperature (plane view and cross-section) is presented in Fig. 2. and Fig. 3.

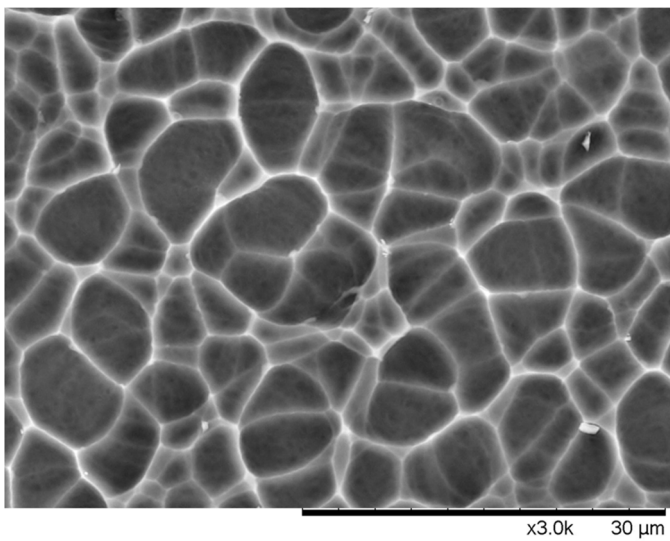


Fig. 2. SEM image (plane view) of multicrystalline silicon wafer with acidic texture obtained at lower temperature – oval pits surface morphology

Surface morphology considerations are, in addition to the anti-reflective layer, crucial for reducing the reflectivity of the solar cell. Decreasing the reflectance results in an increase in the short-circuit current of the cell and therefore, improves power output of PV device. Otherwise, increase of the surface development associated with rising roughness ( $R_a$ ), reduces open

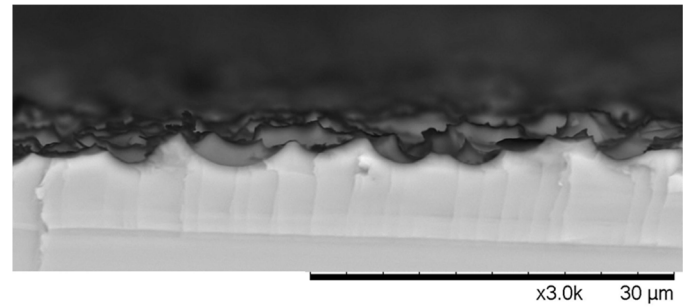


Fig. 3. SEM image (cross-section) of multicrystalline silicon wafer with acidic texture obtained at lower temperature – oval pits and gentle slopes surface morphology

circuit voltage. Unfortunately, in this case surface texturing was a compromise between gaining the best optical and electronical properties. Due to that fact, the surface reflectance and roughness have been compiled and compared.

Atomic force microscopy was applied for roughness determination. The examination was performed for the sample 5 cm × 5 cm but the illustrated area was much smaller: 25 μm × 25 μm using tapping mode. Figure 4 shows selected AFM image, however, the roughness value is the average of at least 10 images.

By the AFM technique it is possible to determine the profile of the object, therefore, pits were analysed in terms of their size, shape and slope. The pits morphology is strongly influenced by the etching process conditions. Nevertheless, the cross-section of the pit is always rounded with typical gentle slope. Any deviations visible in the profile may be associated with an AFM measurement method. The roughness and correlated parameters differ depending on the etching process temperature. The obtained values are shown in Table 1.

TABLE 1

The roughness, skewness, kurtosis of 25 μm × 25 μm mc-Si wafer textured in acidic solution at 10 and 25°C

Solution composition HF:HNO <sub>3</sub> :H <sub>2</sub> O	Temperature of texturization process [°C]	Ra [μm]	Skewness [-]	Kurtosis [-]
8:1:1 vol.	10	0.372	-0.051	2.752
	25	0.925	-0.116	2.513

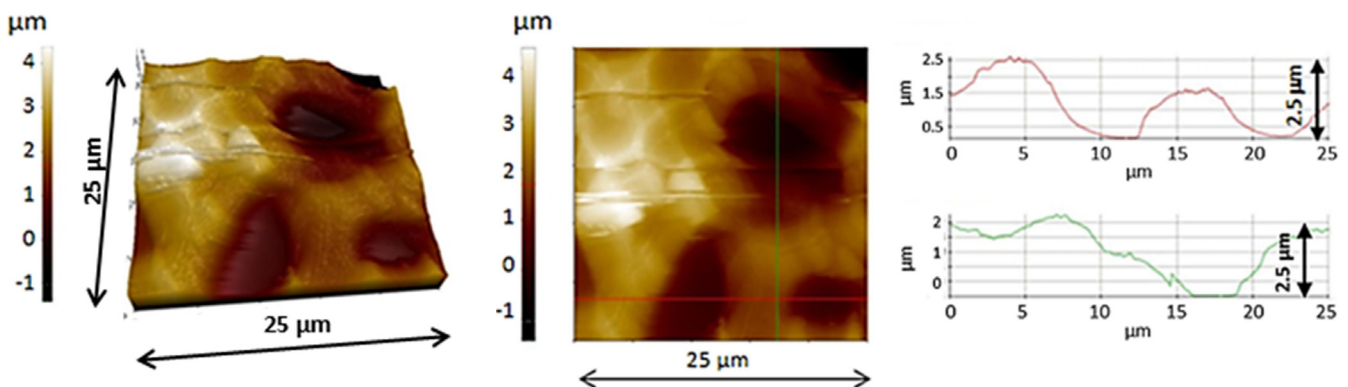


Fig. 4. AFM image and profile of multicrystalline silicon wafer with acidic texture obtained at lower temperature

The roughness of wafers varied due to the temperature changes: Ra decreased along with the temperature lowering. This means a reduction in surface development which, of course, is consistent with the slow reaction mechanism at low temperature. Another interesting parameter is a skewness which illustrates the character of structure. The skewness factors in both cases were negative which means that surface morphology can be described as a hole-like structure. Looking at SEM and AFM images this might be obvious that etched pits structure resembles holes in the wafer. Otherwise, diminishing the etchant temperature increased the skewness value and turned it into positive quantity for temperature below 10°C which represents hill-like structure. Accordingly, the surface of mc-Si wafer still possessed etched pits but their shapes were deep and narrow. For the AFM tip such topography represents silicon wafer morphology after saw cutting with some gaps. Furthermore, it is worth to note that for such a narrow and deep structure, the AFM tip does not fully replicate the shape because it does not reach the bottom of the pit. Therefore, such structures will not be presented. The third parameter – kurtosis describes the homogeneity of surface structures. In this case kurtosis differed insignificantly and can be considered as a constant.

For further investigations wafers with acidic texture prepared at 10°C was selected. For such samples the minority carrier lifetime (after thermal passivation) was higher than for the wafers textured at ambient temperature and equalled to 15.3  $\mu$ s and 10.8  $\mu$ s, respectively. Therefore, it was possible to provide better electrical properties while maintaining good optical properties. At this point, the first step of black silicon formation was completed.

The second step consisted of making wires using the MAE technique with silver as a catalyst. The recipes and etching conditions are described in the ‘Experimental’ section. For the proper characterization of wire sizes, they were previously formed on the chemically polished monocrystalline silicon. The height of wires with relation to etching time is presented in Table 2.

TABLE 2

The average wires height related to the etching time

Etching time	5 sec	10 sec	20 sec	30 sec	40 sec	50 sec	60 sec	5 min	20 min
Average height	180 nm	280 nm	350 nm	460 nm	520 nm	620 nm	890 nm	5 $\mu$ m	14 $\mu$ m

The height as well as plane view morphology and cross-section were analysed by SEM technique. It can be seen that height of wire is approximately linearly dependent on etching time. This is important when the specific length of the wires is required. In Figure 5 plane view of wires with height of about 350 nm (etched in 20 seconds) on polished monocrystalline (Cz-Si) silicon surface is presented.

In this case, wires are visible as a soft porosity. Moreover, heads of wires are close to each other creating, on a first sight, a compact structure. Some light points are not connected with wires, these are tops of pyramids formed earlier during the chemical polishing which were not covered by the wires due to the

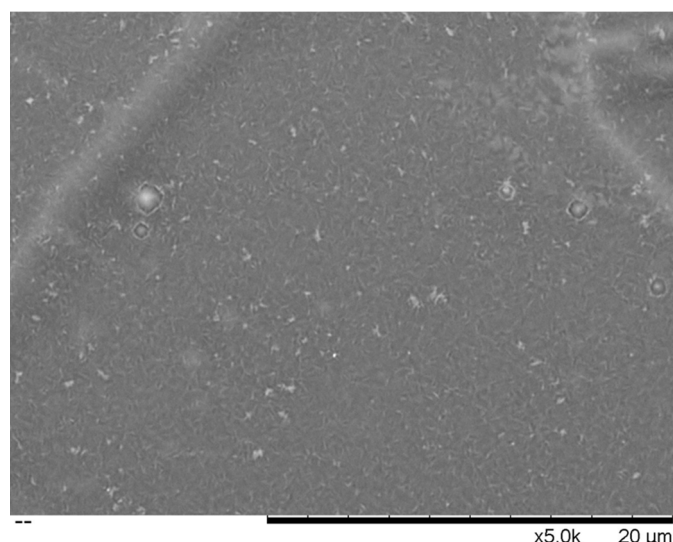


Fig. 5. SEM image of surface morphology of Cz-Si wafer chemically polished with etched (MAE) nanowires for 20 seconds (height of about 350 nm). The plane view shows wires heads

short etching time. For such structures AFM investigations were not carried out. Simply for such rough surface the tip can give unreliable response not entering the space between the wires.

Precise examination of the wires shape, spaces between them and the parallelism of their positions was possible with long wires. The morphology of wire structure for etching time equal to 5 and 20 minutes are shown in Fig. 6.

In the case of long etching time, the contrast in SEM image is high enough to distinguish wires and the spaces between them. Unfortunately, long and thin wires had a tendency to be more fragile and, as a consequence, broke remaining in empty spaces (Fig. 6). Furthermore, the structure was less dense and was not suitable for implementation in solar cell. However, those structures were further investigated because of their excellent optical properties. In Fig. 7 the reflectance spectra in the wavelength range of 300-1100 nm for wires structures with different etching time were shown. The highest reduction of reflectance possessed wafer with wires etched in 5 minutes. This sample behaved like a light trap where the light ray was reflected infinitely times between the wires. Surprisingly, for the sample with longer wires the reflectance was higher. Probably the spaces between wires were wide enough to lose solar radiation coming out from sample and the effective medium did not prohibit the light reflection from the front interface.

For implementation in the solar cells, wires structure should be homogeneous, dense and does not reflect a solar radiation. Because the structures etched very briefly revealed a homogeneous and compact morphology, a series of samples have been prepared and their optical properties were examined. For samples etched for 5, 10, 15 and 20 seconds a reflectance reduction was observed but still remained too high for the texture purposes. Moreover, the occurring interferences caused those structures to behave like a porous layer and not like a texture, which is unwanted. With increasing etching time interferences disappeared and the reflectance decreased significantly to the level of proper texture.



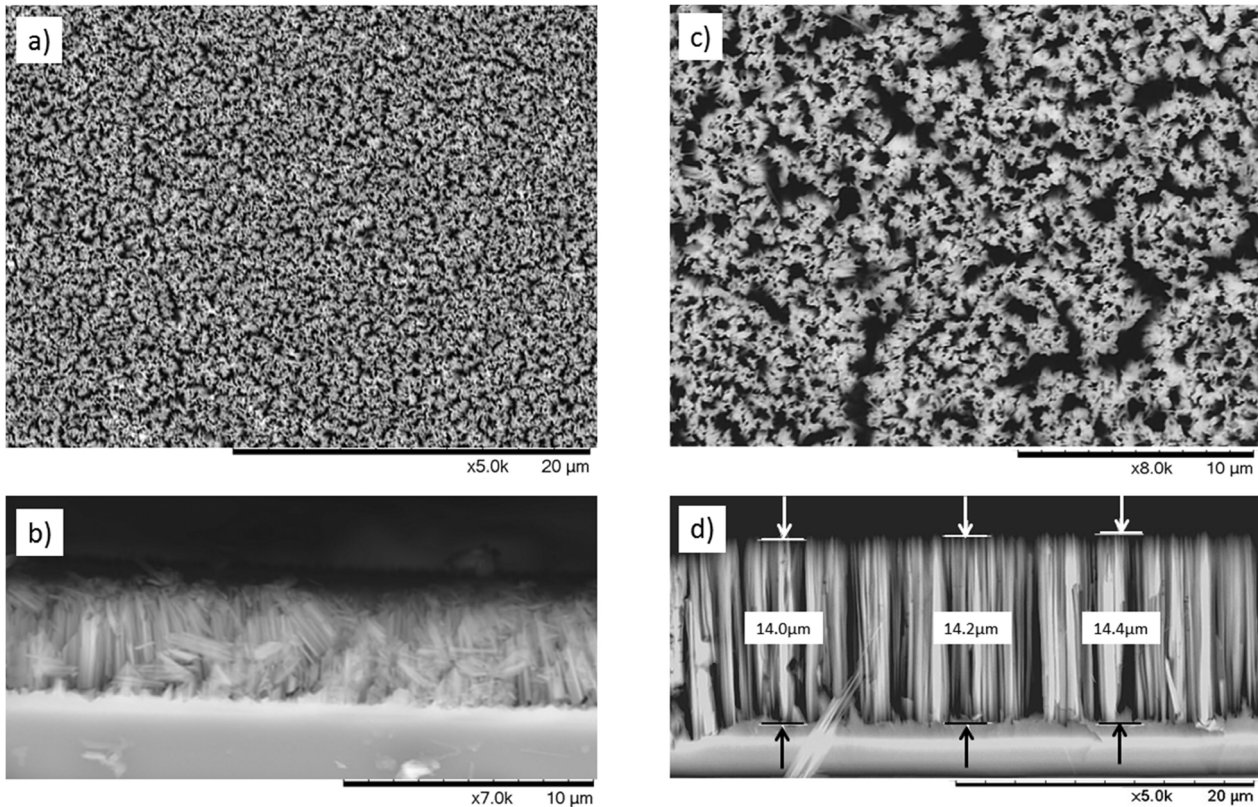


Fig. 6. SEM image of surface morphology of Cz-Si wafers chemically polished with etched (MAE) nanowires for 5 minutes in a) plane view and b) cross-section, and 20 minutes also in c) plane view and d) cross section

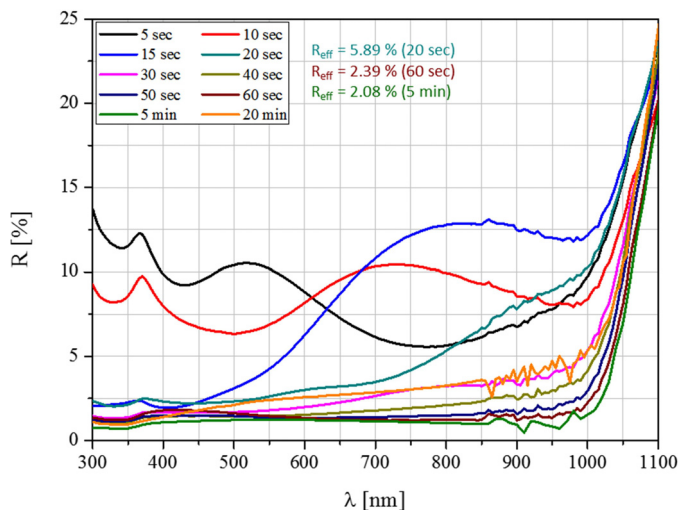


Fig. 7. Reflectance spectra of Cz-Si wafers chemically polished with etched (MAE) nanowires for different time

The wafer etched for 60 seconds demonstrated similar optical properties as the sample treated for 5 minutes. To prove this, the effective reflectance ( $R_{eff}$ ) in the wavelength range 300-1100 nm was calculated according to the formula:

$$R_{eff} = \frac{\int_{300}^{1100} R(\lambda) N_{ph}(\lambda) d\lambda}{\int_{300}^{1100} N_{ph}(\lambda) d\lambda}$$

where:  $R$  – measured total reflectance,  $N_{ph}$  – photon flux.

For example, for a wafer etched for 20 seconds  $R_{eff}$  was equal to 5.89% which is overestimated due to larger tail in the range of 1000-1100 nm. The best samples etched for 60 seconds and 5 minutes have values of  $R_{eff}$  equal to 2.39% and 2.08%, respectively. For both of them, the reflectance reduction was significant and close to the level of black silicon. This led to the conclusion that it is unreasonable to extend the etching time beyond 60 seconds.

The above considerations concerned the wires etched on polished silicon. Traditional acidic texture is characterized by a reduced reflectance, however, the level of this reduction is much more insufficient from the level of black silicon. An attempt was made to combine modified acidic texture and wires structure etched for a very short time. The hypothesis assumes the formation of a surface structure with acidic morphology supported by ultra-short wires etched on the top of pits structure. Figure 8 shows the obtained black silicon structure which was supposed to significantly reduce the reflectance (for the level of black silicon) and simultaneously stayed compact and stable.

The wires are homogeneously distributed on the surface of wafer independently of whether it is the interior of the pit or the outer part of it. Etching process was performed for the same time as for the polished silicon, i.e. 20, 30, 40, 50 and 60 seconds. The microstructure shown in Fig. 8 is characterized by a presence of wires with average height of 350 nm, so the same as for polished silicon (Table 2). This observation is valid for all etching times. At this stage it was found that later solar cell production

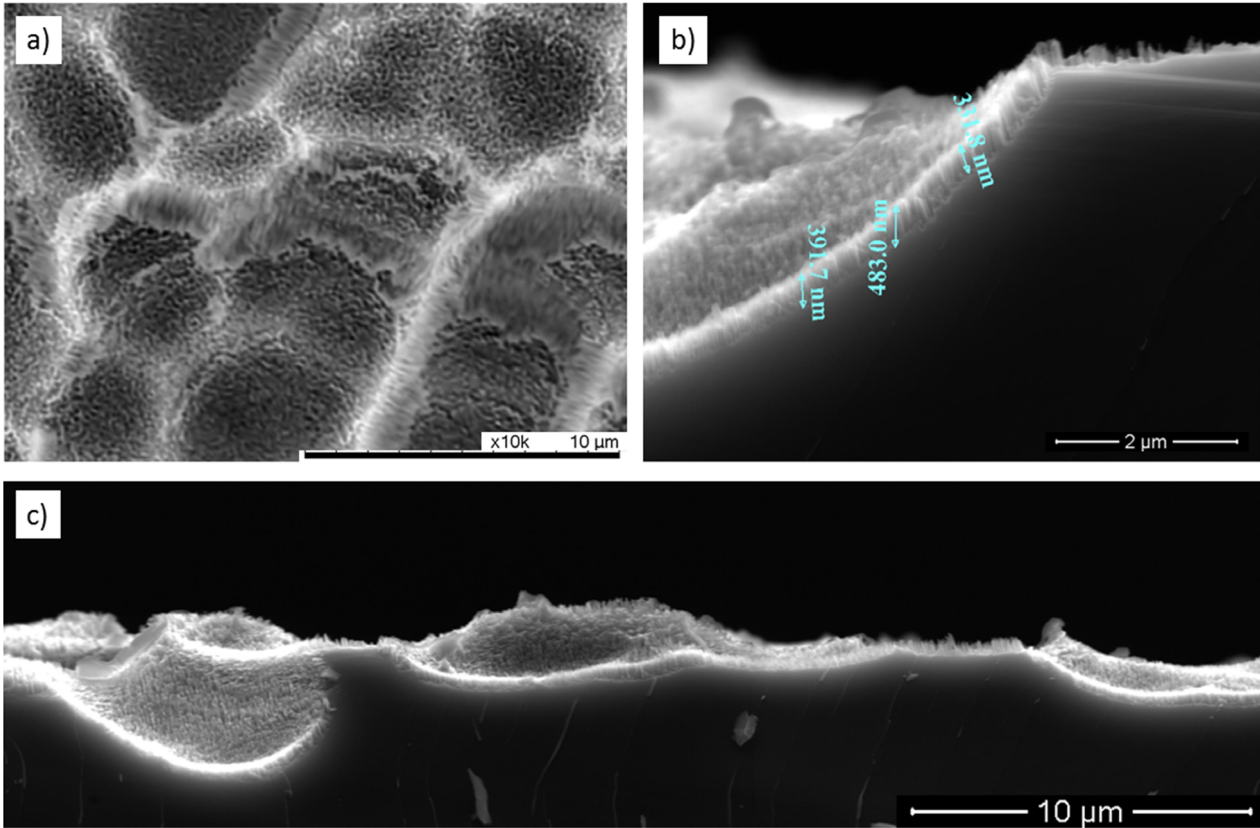


Fig. 8. SEM image of surface morphology of mc-Si wafers texture in acidic solution at low temperature with etched (MAE) nanowires for 20 seconds in a) plane view and b) dimensions in c) cross-section

required wires structure no higher than this average value, despite a potential of further reflectance reduction for higher wires. However, optical testing reveals clearly the different behaviour between the same wires deposited on polished and textured surface. Figure 9 shows reflectance spectrum for the wafer textured at low temperature with wires (green colour) which is low and approximately constant in the whole wavelength range, except last part for high wavelength. This is characteristic for all the samples due to low silicon absorption region which, in principle,

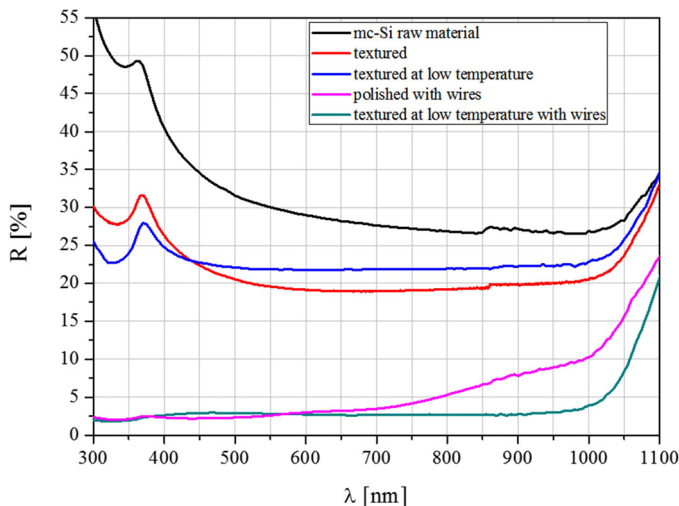


Fig. 9. Reflectance spectra of mc-Si wafers texture in acidic solution at low temperature with etched (MAE) nanowires

is negligible through low contribution to quantum efficiency. The  $R_{eff}$  value was found to be 3.65% which is lower than for the polished sample only with wires (pink colour) with  $R_{eff}$  at level 5.89%. This means that combining two types of surfaces modifications is justified in terms of obtaining a good quality texture with a very low reflectance.

Moreover, applying a modification in acidic texturing i.e. lowering process temperature, the electrical properties were improved (increase in minority carrier lifetime) while maintaining good optical performance. This is probably a consequence of slower etching reaction which provide to the structure with lower roughness and, therefore, lower surface recombination. Figure 9 shows reflectance spectra for mc-Si textured at ambient (red colour) and low temperature (blue colour) which are comparable in  $R_{eff}$  values equalled to 20.70% and 22.76%, respectively.

After achieving satisfactory results in the implementation of wires for the polycrystalline wafers texturing in acidic solution, it was decided to take further tests. Thus, wires were etched in the same way on the surface of monocrystalline silicon typically etched in alkaline solution. Wires with the same average height of 350 nm were performed on the pyramidal structure what are shown in Fig. 10.

Homogeneous structure of wires was present mostly on the entire surface of pyramids. However, in some places, especially on the tops of the highest pyramids, it can be seen that etched wires are shorter or completely worn out. This means that the wires are not so stable mechanically on the pyramid texture.



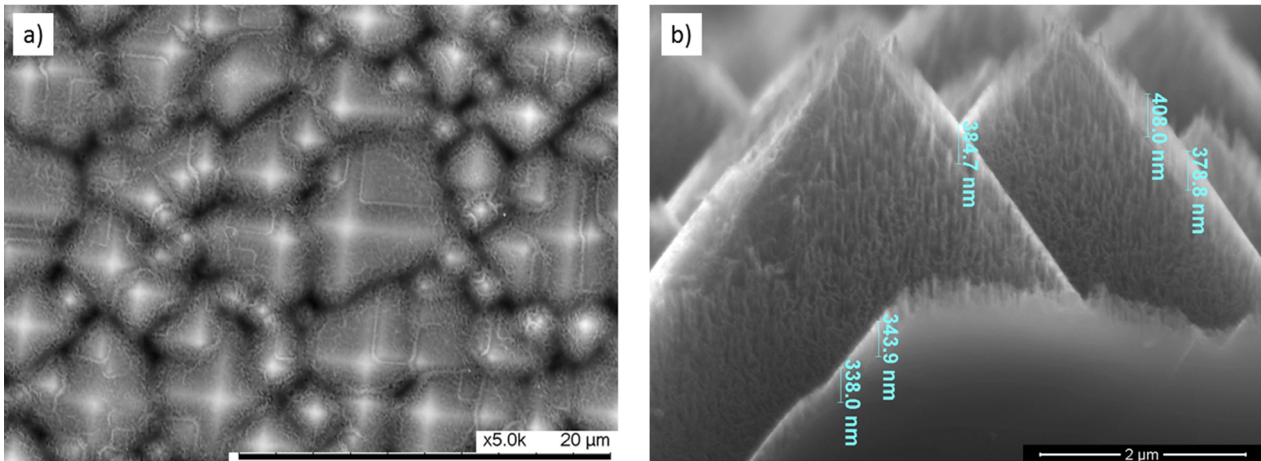


Fig. 10. SEM image of surface morphology of Cz-Si wafers texture in alkaline solution at elevated temperature with etched (MAE) nanowires for 20 seconds in a) plane view and b) cross-section

This statement is proved in the reflection measurement. The reflectance spectra are shown in Fig. 11.

The presented spectra show reflectance reduction with increasing time of wires etching. However, the same time of wires etching, equal to 20 second, resulted in the  $R_{eff}$  value higher (4.00%) than for the wires obtained on pits after acidic texture (3.65%). Of course, the difference is not great, but the fact is that the wire structure is more amenable to damage if it is present on exposed pyramids in opposite to the position inside of hidden pits. In spite of this, the formation of wires on the textured surface (black silicon as a two-step texture) always lowers the reflectance of the typical one-step textured surface. In addition, in each case, the reflectance from the two-step textured surface is lower than for the wire structure etched on the polished surface.

Although further solar cell production steps are not taken into consideration in this publication, but the Authors wish to suggest some of the problems involved in the implementation of

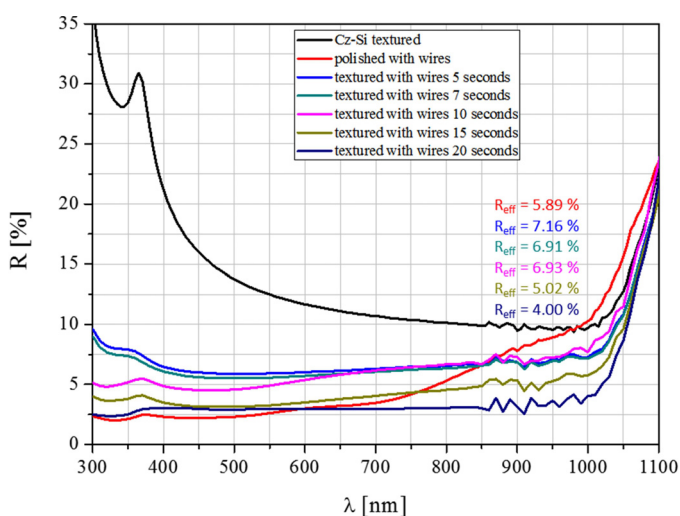


Fig. 11. Reflectance spectra of Cz-Si wafers texture in alkaline solution at elevated temperature with etched (MAE) nanowires for different time

the two-step texture. The height of the wires should be adjusted to the depth of the junction. If the wires are formed before the diffusion process, it is important to consider which size they should possess in order not to be destroyed during the dopant application or to be consumed at high temperature processes. If wires are etched on wafers with p-n junction, their height should be low enough to not consume the entire dopant in the etching process. Also it should be remembered that in such situation the junction depth will be reduced which will affect the electrical properties of the solar cell. An interesting solution can be an application of the liquid dopant source described in [43]. It seems also possible to use an admixture source with a very high concentration of phosphorus, which preparation and spray-on method are described in [44]. Moreover, it is important to have good surface passivation to provide high minority carrier lifetime for a wafer which is characterized by very high roughness described in [38]. And last but not least, it is difficult to form metallic contact on such rough structure. Typical screen-printing, described in [45-46], provides to the fingers peel-off with wires as soon as the contact is fired. This is due to the insufficient penetration into the spaces between the wires and temperature stress during the firing and cooling. This means that other techniques of metallic contacts forming are required. Authors consider the possibility of etching paths for metallic contacts deposited by screen-printing method. Other ways of electrodes formation, taking into consideration, are making contacts by replacing silver with another metal or reinforced silver with embedded copper [47-48]. All investigations should be supported by electroluminescence measurements [49].

#### 4. Conclusion

It has been demonstrated that the proposed two-step short wet etching is applicable for mc-Si wafers and allows black silicon formation. Moreover, in the first step an acidic texture at low temperature of 10-12°C was performed. By this treatment

the reactivity of process was changed and therefore, better optical and electrical properties were obtained. The second step was based on wires formation by MAE technique with Ag as a catalyst. The height of wires was examined (on chemically polished Cz-Si) and a linear dependence of height vs. etching time was denoted. The optimal wire height was set at the level of 350 nm (etched for 20 seconds) which resulted in the  $R_{eff}$  value equal to 3.65% (combined with acidic pits texture), 4.0% (combined with alkaline pyramidal texture) and 5.89% (on chemically polished surface) in a wavelength range of 300-1100 nm. The obtained structure of black silicon had a best optical properties compared to typical one-step wet texture or wires formed on the non-textured surface.

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